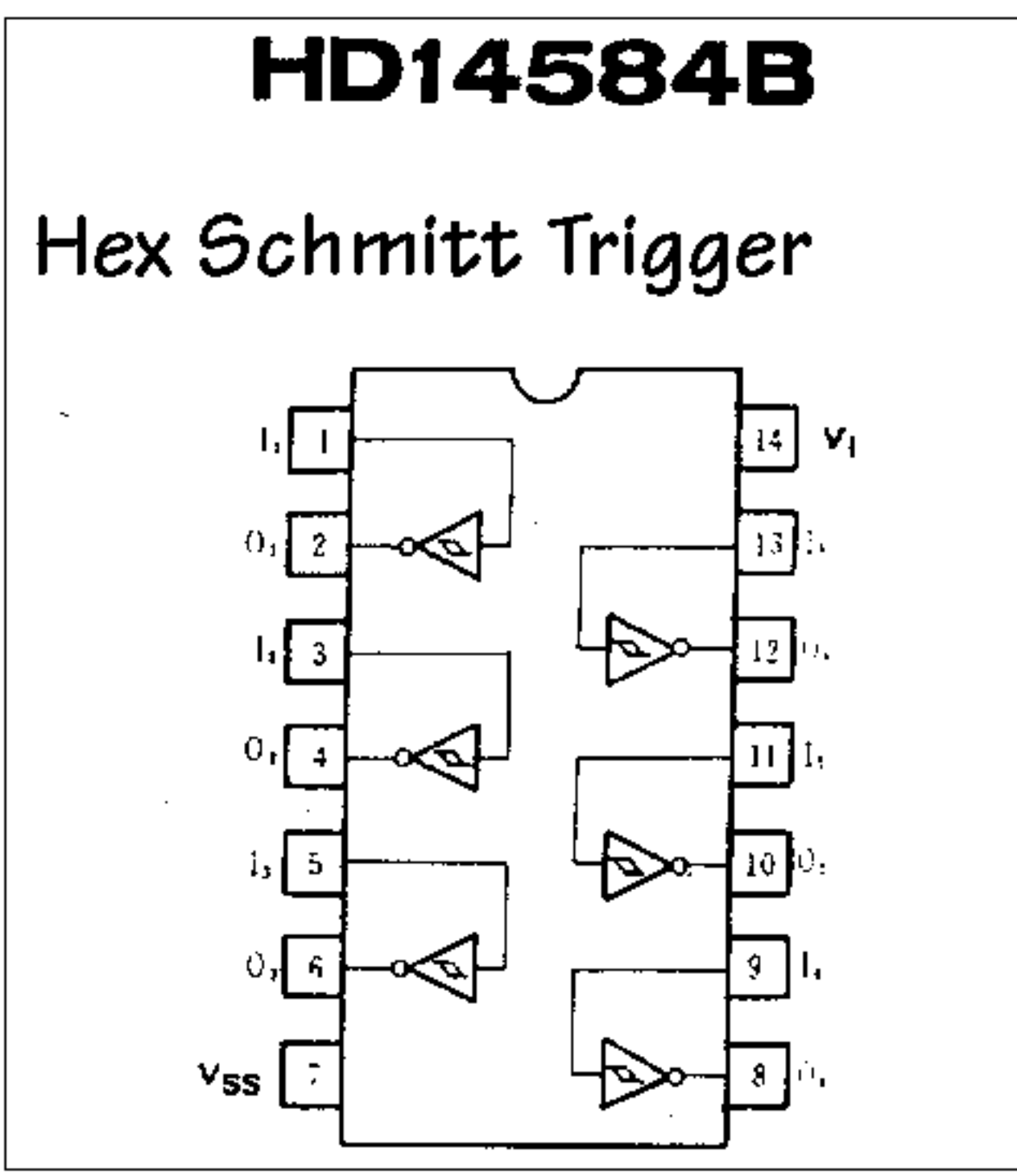
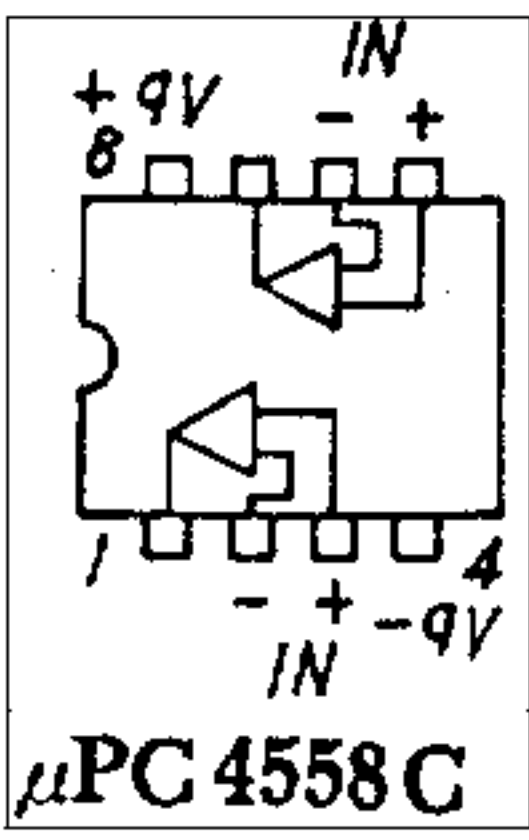
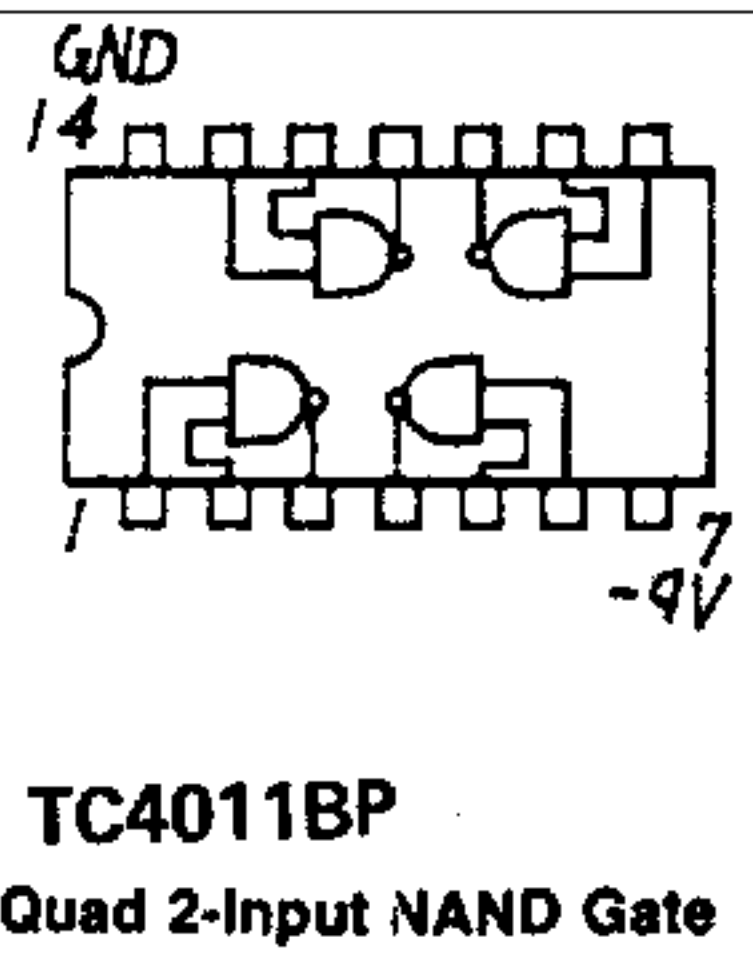
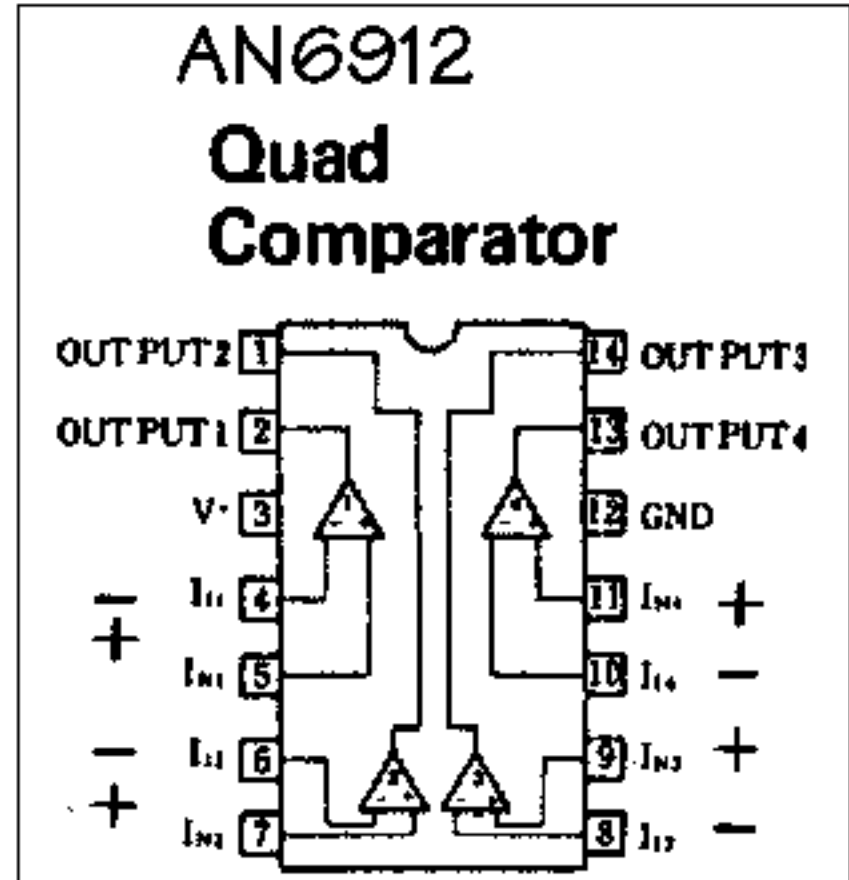
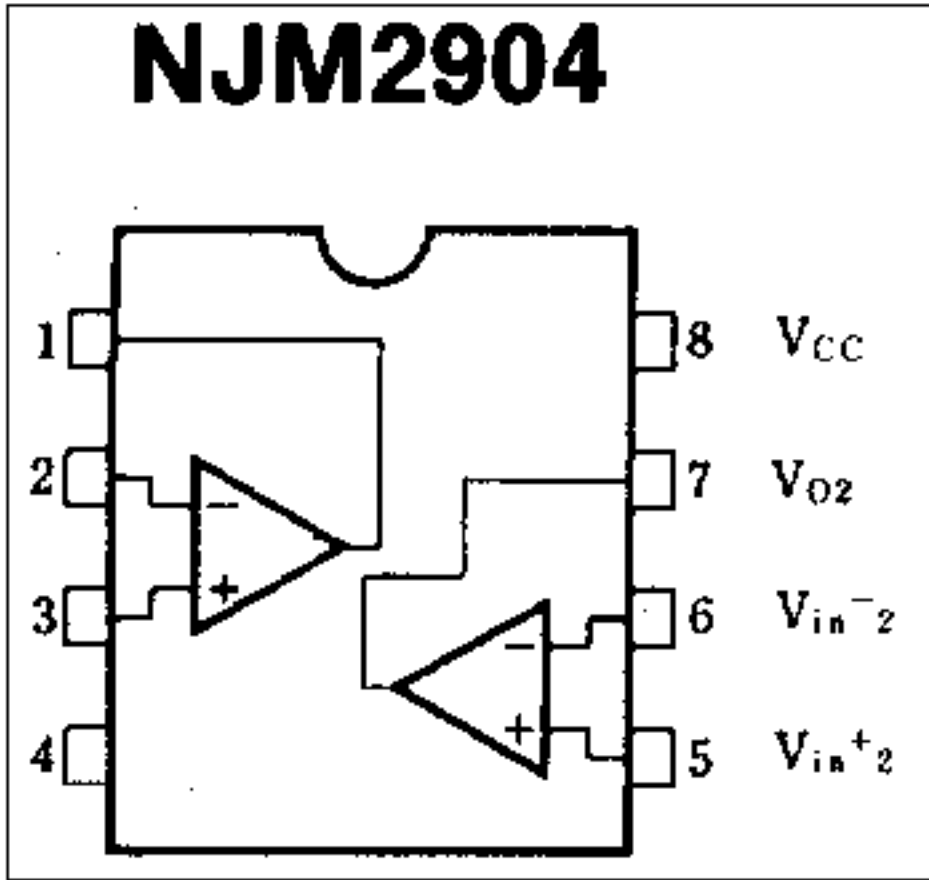
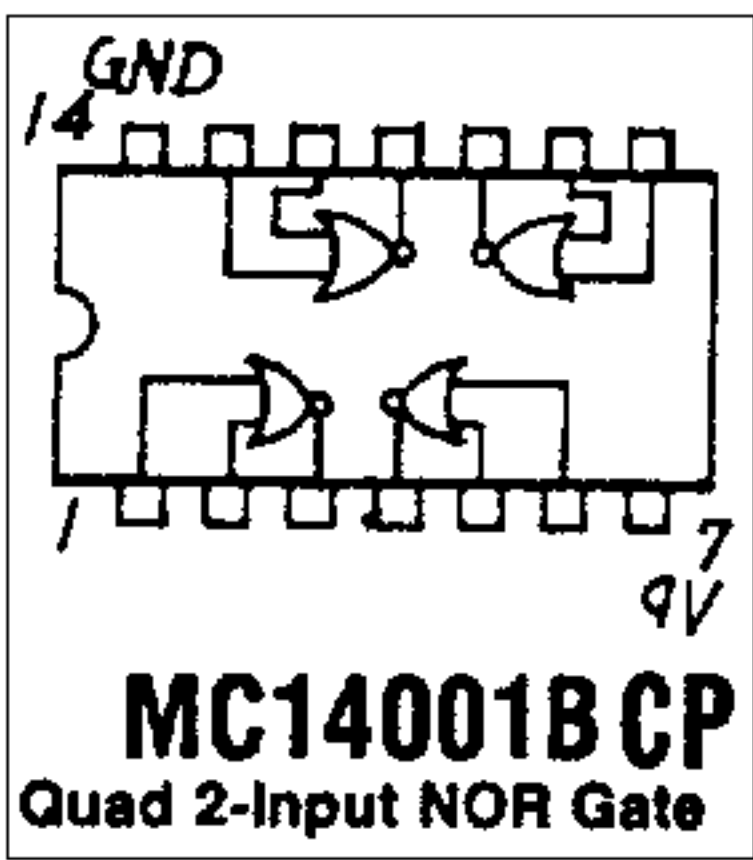




MC14013B

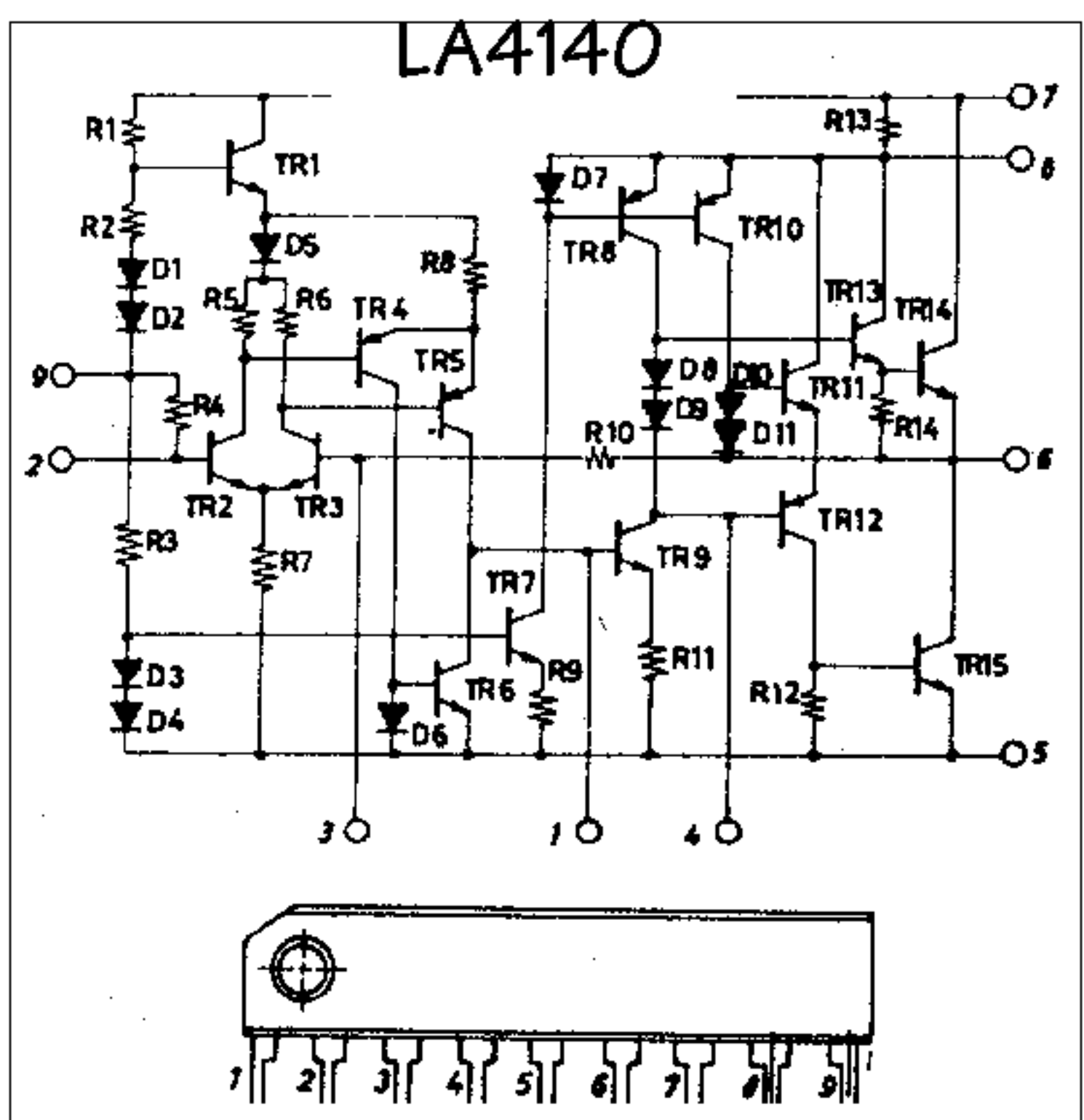
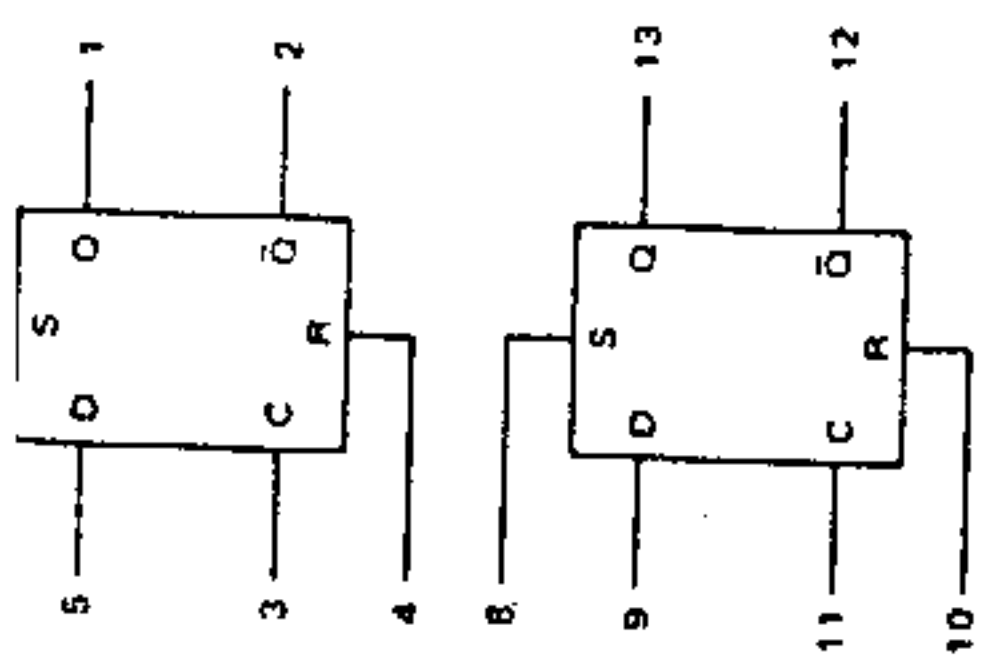
DUAL TYPE D FLIP-FLOP

TRUTH TABLE

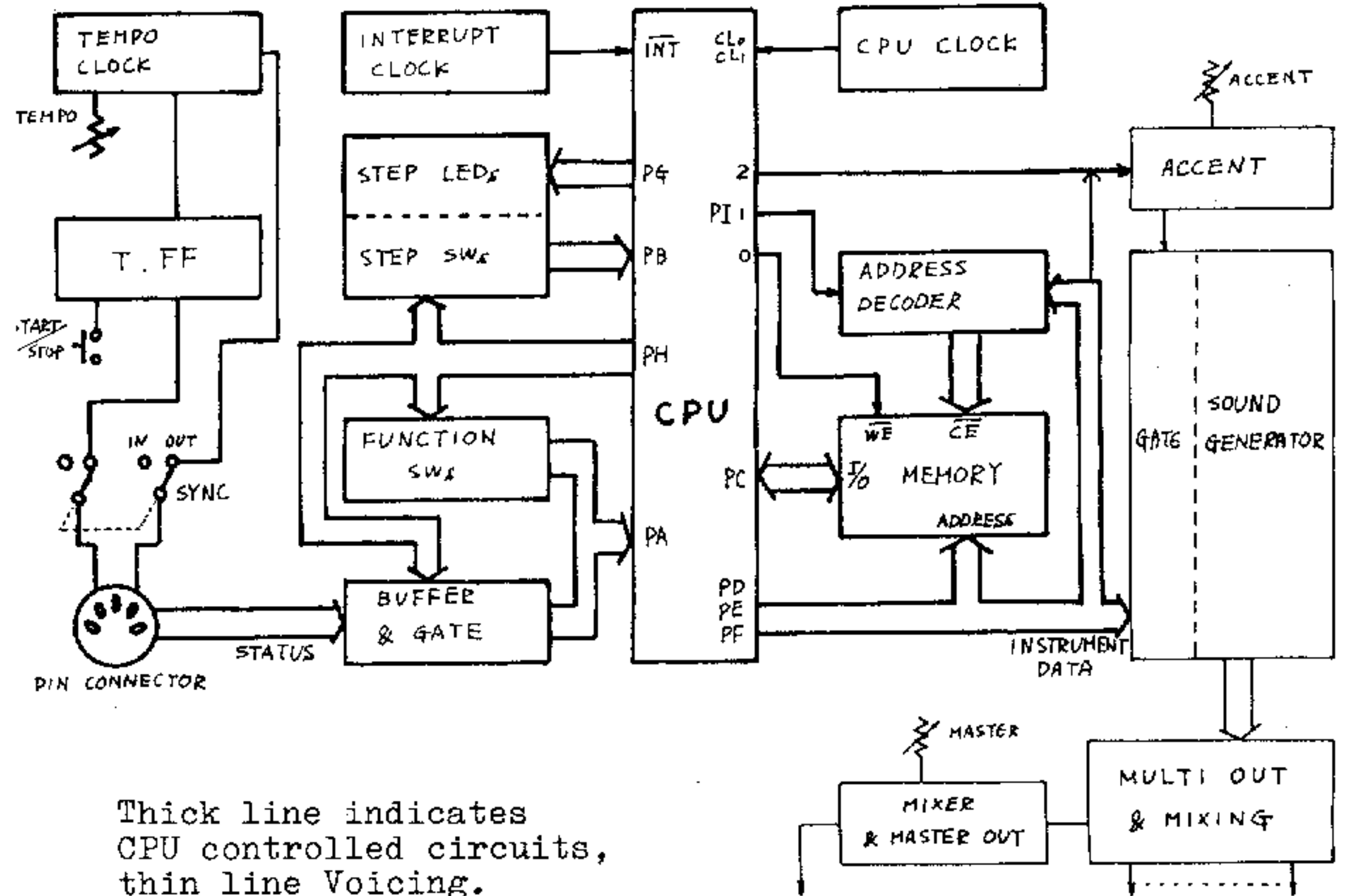
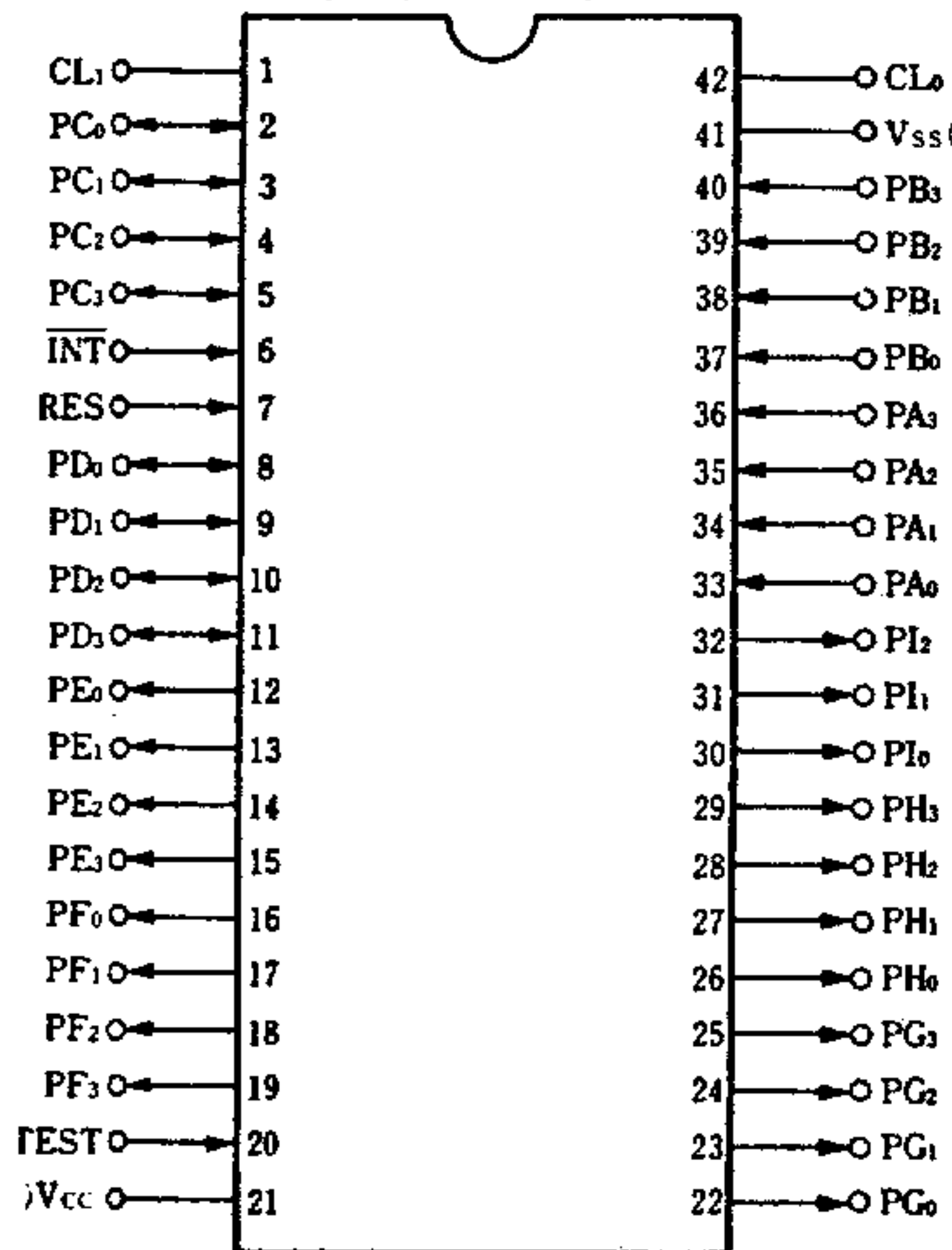
INPUTS				OUTPUTS	
CLOCK ¹	DATA	RESET	SET	Q	$\bar{Q}$
	0	0	0	0	1
	1	0	0	1	0
	X	0	0	Q	$\bar{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

X = Don't Care
1 = Level Change

No Change



μPD650C (Top View)



BLOCK DIAGRAM

μPD650C-085 FUNCTIONAL DESCRIPTION

No.	No.	
PH (Port H)	0	26
	1	27
	2	28
	3	29
PA (Port A)	0	33
	1	34
	2	35
	3	36
PB (Port B)	0	37
	1	38
	2	39
	3	40
PG (Port G)	0	22
	1	23
	2	24
	3	25
PE (Port E)	0	12
	1	13
	2	14
	3	15
PD (Port D)	0	8
	1	9
	2	10
	3	11
PF (Port F)	0	16
	1	17
	2	18
	3	19
PC (Port C)	0	2
	1	3
	2	4
	3	5
PI (Port I)	0	30
	1	31
	2	32

Scanning signal outputs to switches
Switching signal outputs to STATUS BUFFER & GATE

Switch scanning signal inputs
STATUS (TEMPO CLOCK, START/STOP, TAP) inputs

Inputs from STEP Switches (RHYTHM SELECT Switches)

Drive signals to STEP LEDs

I/II Memory bank select
MEMORY ADDRESSES
These pins use CE from ADDRESS Decoder to select cells in RAM to be accessed
INSTRUMENT DATA
These data need COMMON TRIG to trigger Sound Generators being designated

LT SD BD AC
Step numbers

Data Inputs/Outputs

Memory WE
Memory CE (associated with PE-2, 3 at ADDRESS DECODER)
Trigger Pulse (INSTRUMENT) output

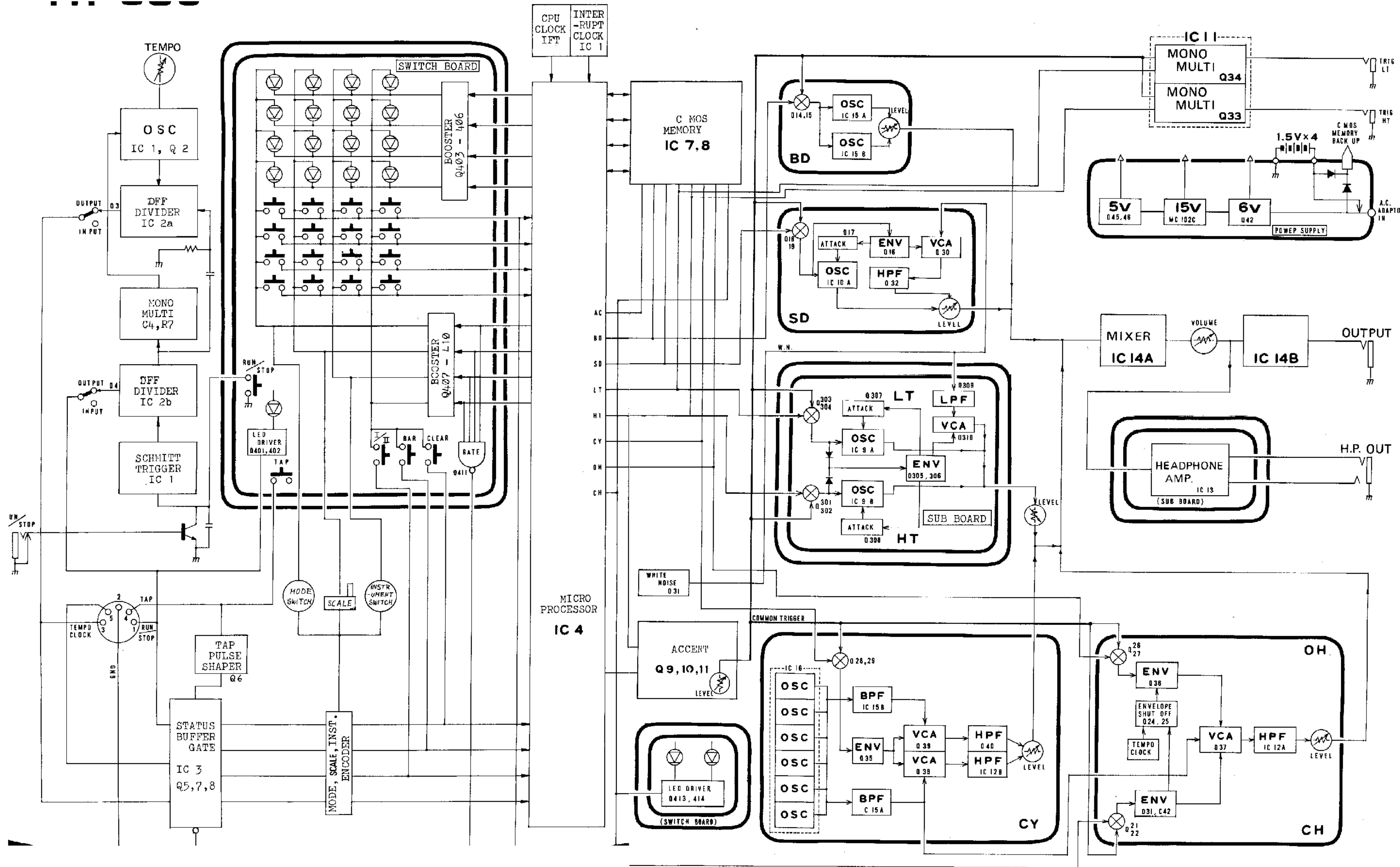
581-484C
(PCB 291-494C)

521-424C

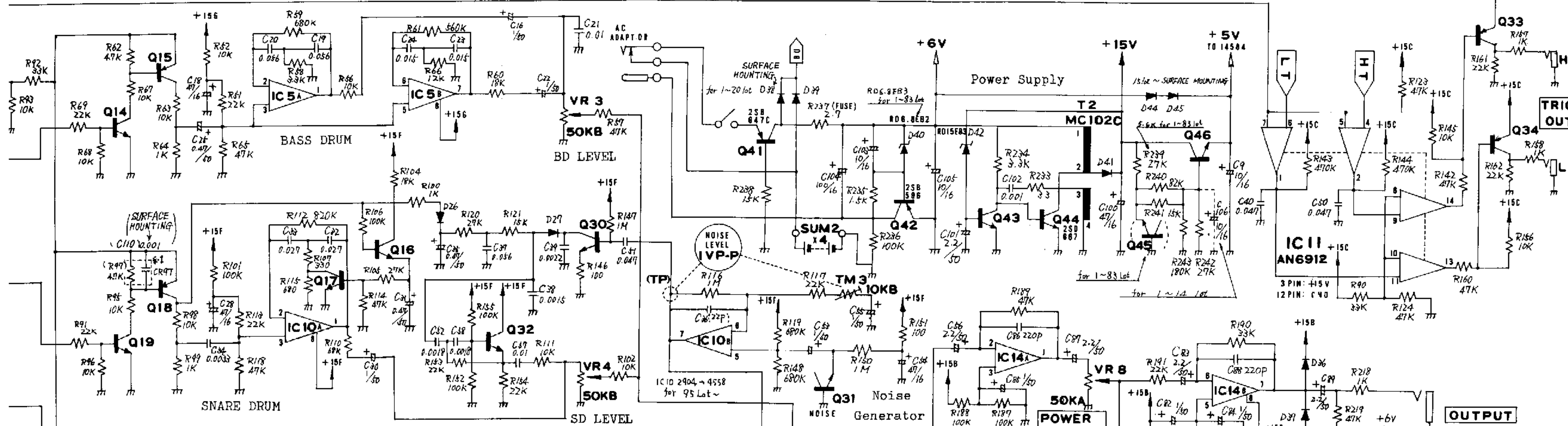
(PCB 291-494C)

(PCB 291-492C)

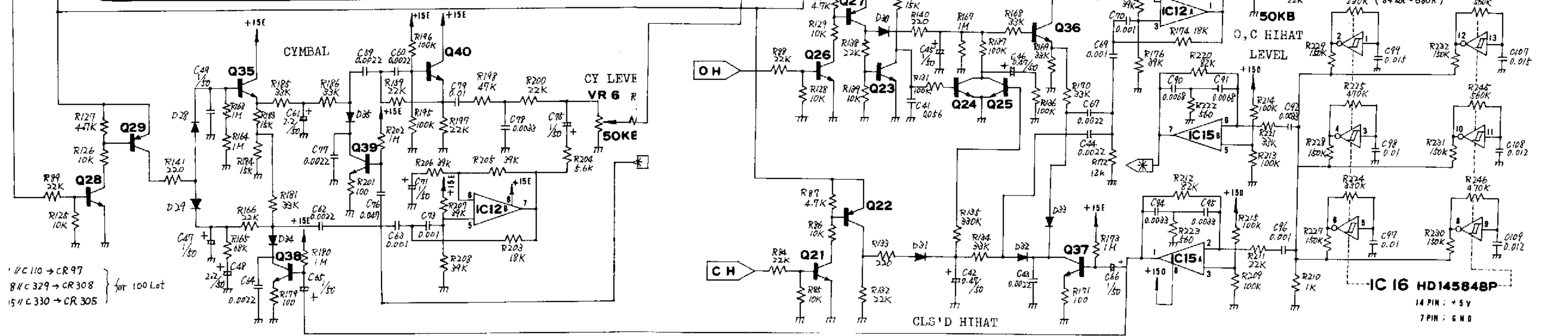
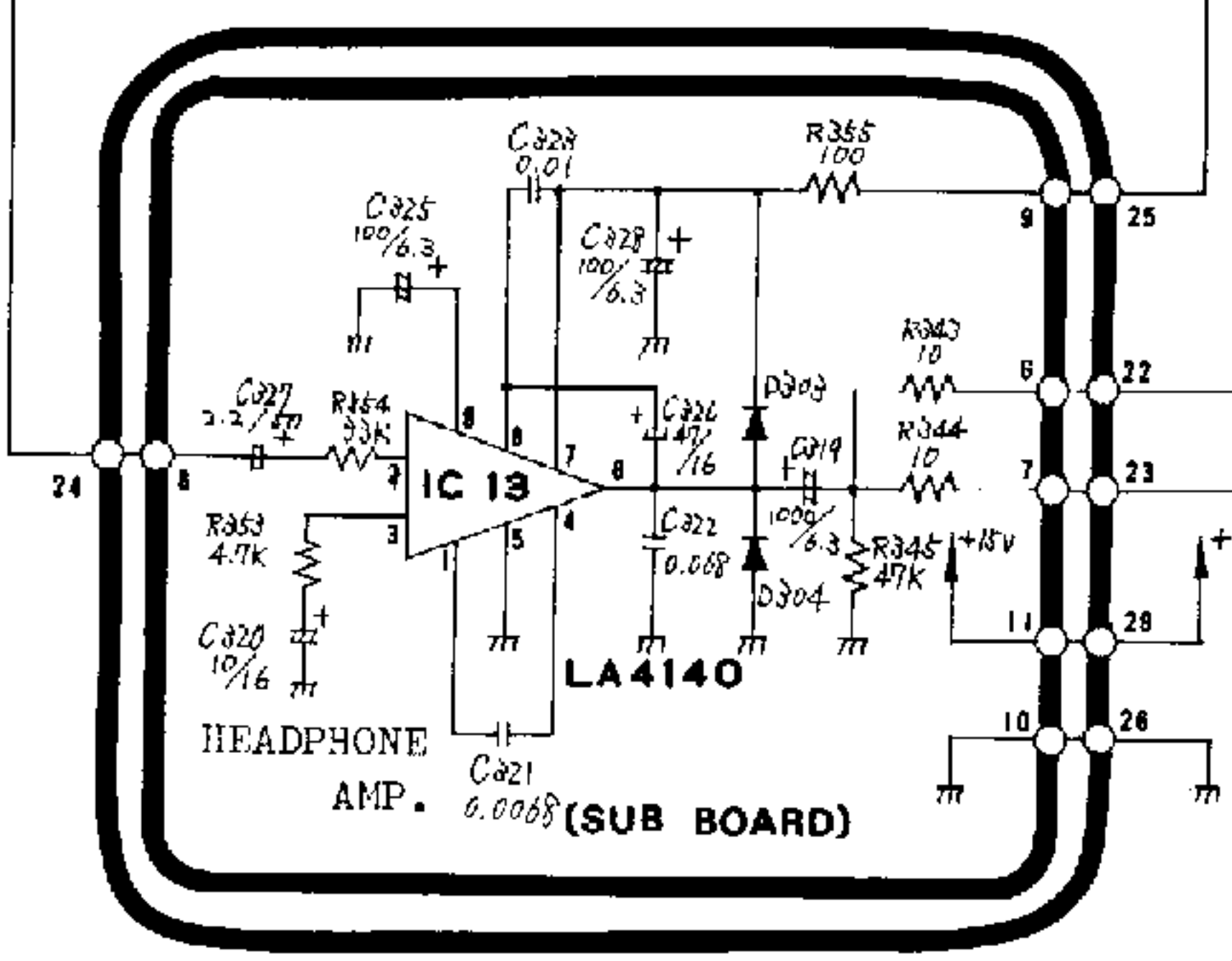
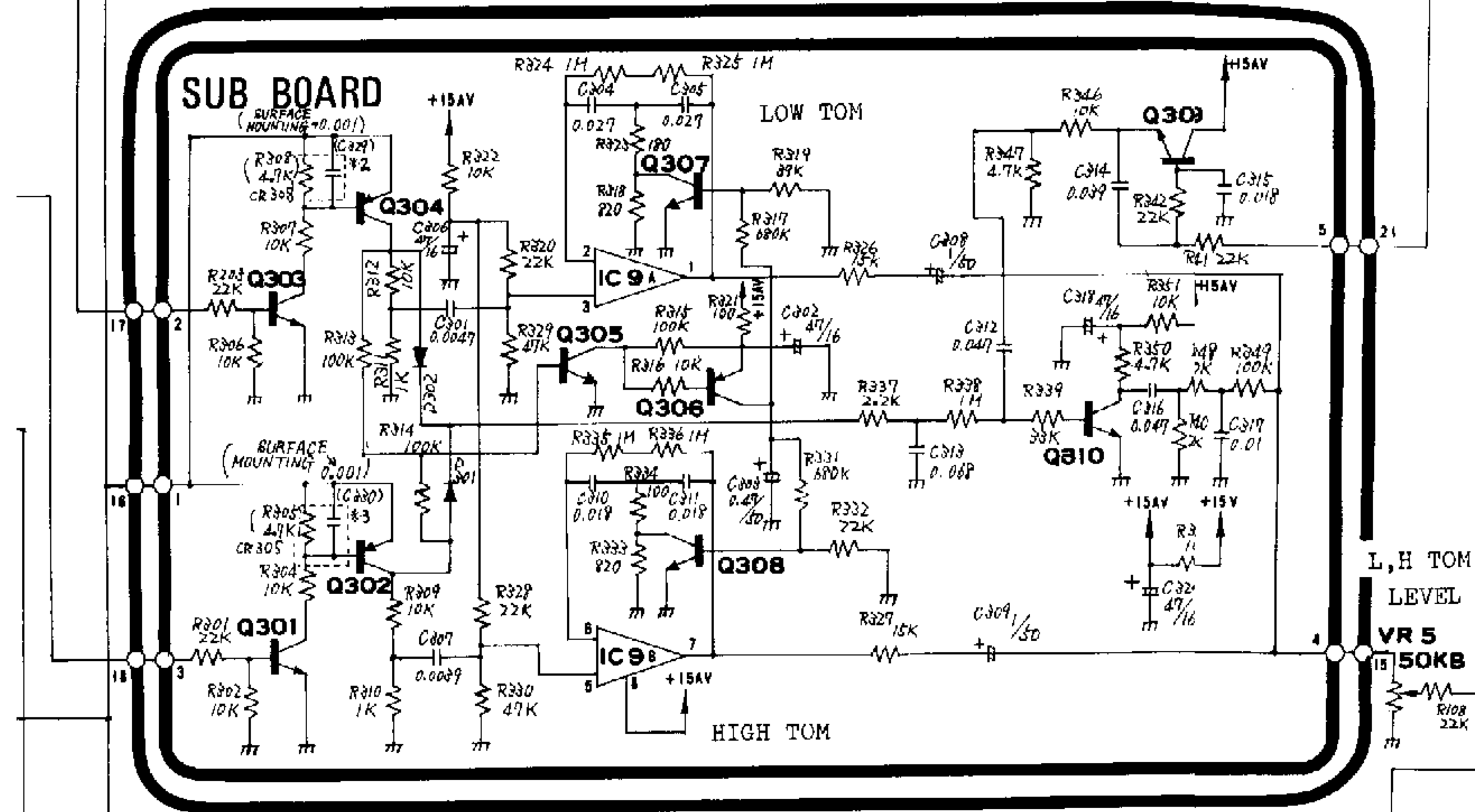
(PCB 291-492C)



MAIN BOARD



SUB BOARD



ALL NPN TRANSISTORS ON THE MAIN BOARD AND THE SUB BOARD ARE 2SC945

ALL PNP TRANSISTORS ON THE MAIN BOARD AND THE SUB BOARD ARE 2SA733

ALL NPN TRANSISTORS ON THE SW. BOARD ARE 2SC202

ALL PNP TRANSISTORS ON THE SW. BOARD ARE 2SA937

ALL DIODES ARE 1S2473

ALL OP AMP'S ARE JRC2904 IC15 uPC4558

1/4 C110 → CR97
8/4 C329 → CR308
15/4 C330 → CR305